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Mathias Wendt

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Please find below and/or attached an Office communication concerning this application or proceeding.

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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 10/585,368
Filing Date: July 05, 2006
Appellant(s): WENDT ET AL.

William S. Francos, Reg. No. 38,456
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed September 29, 2009 appealing from the Office action mailed April 7, 2009.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

2005/0275386	Jepsen, et al	12-2005
5,546,065	Vinciarelli et al	8-1996

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6,771,052	Ostojic	8-2004
5,809,256	Najemy	9-1998

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-19 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. Claim 1 and 10-11 contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification does not describe how a person of ordinary skill in the art would be able to construct a DC/DC convert that does not buffer energy, as discussed above. The specification recites the preferred embodiment in which the DC/DC converters do not contain capacitors. This configuration, however, is not equivalent to the broad limitation that the DC/DC converters do not buffer any energy at all. Claims 2-9 and 12-19 depend from claims 1 and 10, and are rejected under §112(1) as well.

For the purpose of the art rejection of the claims, the claim will be interpreted as reciting that the converters to not comprise capacitors.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-3, 8-13 and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jepsen (US 2005/0275386) in view of Vinciarelli (US 5,546,065).

With respect to claims 1 and 10, Jepsen discloses a decentralized power generation system (fig 1; par 43-44) and the associated method, comprising: a plurality of decentralized power generating units (FC, PV); a plurality of DC/DC converters (A) connected to another one of said power generating units and, when a voltage supplied from a respective power generating unit meets or exceeds a threshold voltage (obvious), the associated DC converter is configured to convert a current provided by said power generating units; a DC bus (3); and at least one power receiving component (B) connected to the DC bus, wherein the power receiving component is physically separated from said DC/DC converters.

The DC/DC converter will not have any power to convert when a source is not supplying any power (during nighttime). The “threshold voltage” of Jepsen is interpreted as zero (0) volts. With zero volts, the power input to the converter is also zero ($P = V * I$). Once a source begins to actually supply power (par 43, lines 1-5), the converter will then convert a current supplied by that source.

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Further, all of the components are physically separated from each other, as is illustrated by borders and spacing between components (fig 1). Jepsen also clearly discloses that there is a DC bus between the converters (A) and the inverter (B).

Jepsen discloses that the DC/DC converter comprises a transformer and two capacitors (fig 3, items 9 and 16). Jepsen further discloses that the DC/DC converter is in fact comprised of a DC/AC inverter (18) and an AC/DC rectifier (14)(par 52). One skilled in the art would recognize that it would not be necessary to convert input DC power to an intermediate AC value in order to provide DC output power.

Vinciarelli discloses a DC/DC converter (fig 2; col. 7-9) that is comprised of a transformer and does not contain a capacitor. Jepsen and Vinciarelli are analogous because they are in the same field of endeavor, namely DC/DC converters comprising transformers. At the time of the invention by applicants, it would have been obvious to replace the DC/AC and AC/DC converters disclosed in Jepsen with the DC/DC disclosed in Vinciarelli in order to reduce the number of parts in the converter.

With respect to claim 11, Jepsen and Vinciarelli disclose the limitations of claim 1 and Jepsen further discloses controlling the output voltage of the converters not to exceed a predetermined value (par 18-19).

With respect to claim 2, Jepsen discloses the converters operate autonomously (par 4, 44).

With respect to claims 3 and 13, it would be obvious to one skilled in the art that a “mechanical connection” exists between the power sources and the converters, which are already physically connected by an electric transmission line.

With respect to claims 8 and 18, Jepsen discloses said power receiving component is an inverter to feed AC current into an AC power supply system (13).

With respect to claims 9 and 19, Jepsen discloses each of said power generating units comprises at least one photovoltaic module (PV). Jepsen discloses (par 43, lines 19-21) that the power sources are photovoltaic cells and that they may be other types of sources in other embodiments.

With respect to claim 12, Vinciarelli discloses a DC/DC converter without electrolyte capacitor, as discussed above.

5. Claims 4-6 and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jepsen in view of Vinciarelli and Ostojic (US 6,771,052).

With respect to claims 4 and 14, Jepsen discloses a microcontroller on the power receiving component, but does not expressly disclose the microcontroller is adapted to survey a voltage on said DC bus and to reduce the power retrieved from said DC bus when the voltage on said DC bus is detected to be decreasing. Ostojic discloses a multiple-output DC/DC power supply with a microcontroller programmable to monitor the voltage of a bus and to react accordingly in the presence of a fault, which may be a reduction of power in the bus due to failure of one of the converters (col. 7, line 63 to col. 8, line 18).

Jepsen and Ostojic are analogous because they are from the same field of endeavor, namely microcontroller controlled converters. At the time of the invention by applicants, it would have been obvious to modify the Jepsen and Vinciarelli converters with the Ostojic microcontroller in order to increase the protection level of the system.

With respect to claims 5 and 15, Ostojic discloses the microcontroller is able to ramp-up and ramp-down the DC/DC converters besides controlling the sequence for turning on (col. 6, lines 48-62).

With respect to claims 6 and 16, Jepsen discloses at least one plug connection (darkened circles at the top of each converter) for electrically connecting a respective converter in common to said DC bus and, via said control line (5), to said at least one power receiving component (B).

6. Claims 7 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jepsen in view of Vinciarelli, Ostojic and Najemy (US 5,809,256).

Najemy discloses a power switching converter with connector pins for power and data, wherein the pins for power are longer than the pins for data (col. 5, line 52 to col. 6, line 25). Jepsen, Vinciarelli, Ostojic and Najemy are analogous because they are from the same field of endeavor, namely converters. At the time of the invention by applicants, it would have been obvious to modify the Jepsen pins as shown in Najemy such that, during plug insertion/removal, selected pins are connected/disconnected first (Najemy; col. 2, lines 33-46).

(10) Response to Argument

The issue of section headings is not germane to the art rejection of the claims. While sections headings may not be required by the MPEP, they do provide a guide to help readers find information within the specification.

The Examiner maintains that the §112(1) rejection of the claims is proper. Appellants have quote a portion of the specification (Brief, page 6) in which they

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describe how the DC/DC converters do not require electrolyte capacitors. The Examiner does not challenge the physical description of constructing a DC/DC converter without a capacitor or the stated benefits of such a design. Such a configuration is possible and would be a proper claim limitation. It is respectfully noted that if appellants had claimed a plurality of DC/DC converters without capacitors, the §112(1) rejection would not have been presented.

Appellants' specification states, "The presented PV power plant has further the advantage that the DC/DC converters 31, 32 required basically no buffering of energy" (emphasis added; specification, page 11, lines 1-2; Brief, page 6). The specification's disclosure of "basically no buffering of energy" does not provide support for the limitation regarding the plurality of DC/DC converters, "none of which are configured to buffer energy."

First, the plain language of the specification, which states "basically no buffering of energy," is not equivalent to the claim language of "none of which are configured to buffer energy." Appellants' use of the word "basically" infers some nominal amount of energy buffering. Thus, there is no written description in the specification for constructing a DC/DC converter which does not buffer any energy.

Second, as discussed above, appellants have stated and described the benefits of not using capacitors in a DC/DC converter. The claims, however, actually recite the benefit associated with not using capacitors, as opposed to the physical act of not including the capacitors. While the Examiner admits that capacitors buffer energy, they are not the only components that do so. The Examiner submits that almost all electrical

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devices buffer energy to some extent. For example, the fact that the DC/DC converter takes up physical space means that it buffers some energy. At any one moment in time, the voltage and current at the output of the converter are not exactly the same as the voltage and current at the input. If current is applied to the input of a DC/DC converter, some time is required (albeit a miniscule portion of a second) for a given electron within the current stream to be processed and provided at the output. This time delay is a buffer. And since the buffer involves voltage and current (and therefore, power), it is also an energy buffer.

By reciting that the DC/DC converters do not buffer energy, appellants' have actually excluded almost every electrical component (not just capacitors) from the converter. For example, a component as simple as a resistor also buffers energy. A resistor functions to slow the passage of electrons. This function has a side effect of producing a voltage drop across the resistor as well ($V=IR$). By slowing the passage of current and by altering the voltage potential, the resistor buffers energy. The current value at the resistor output is delayed in time and reduced in value from the input current. Thus, appellants' claims are equivalent to reciting that the DC/DC converters have no resistance. There is no support for this function in the specification.

Appellants' have provided no written description in the specification to allow one skilled in the art to construct a DC/DC converter which does not buffer any energy. Appellants have discovered a benefit to not using capacitors in the DC/DC converters. The §112(1) rejection is proper because appellants have claimed removing the benefit

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of excluding capacitors (basically no energy buffering), instead of the limitation of physically excluding capacitors.

As stated at the end of the §112(2) rejection (see above), “[f]or the purpose of the art rejection of the claims, the claim will be interpreted as reciting that the converters do not comprise capacitors.” Appellants have not shown how to construct a DC/DC converter that does not buffer any energy. The specification, however, does indicate that the desired embodiment of the DC/DC converter does not include a capacitor. Therefore, the Examiner believes there is supported for the interpretation of the claim language used in the art rejection of the claims.

Regarding the art rejection of the claims (Brief, beginning at page 8), appellants have selected claim 10 as a representative of the three independent claims (1, 10, 11). Appellants’ first argument focuses on the limitation of buffering energy (page 8 to the first sentence of page 9). The Examiner admits that Jepsen discloses a DC/DC converter with a capacitor (Jepsen; fig 3, items 16 and 9). As discussed above, all components buffer some energy. Therefore, appellants’ statement (Brief, first sentence of page 9) is incorrect. Since Jepsen discloses a DC/DC converter with a capacitor, the §103 rejection of the claims relied on a secondary reference, Vinciarelli, as will be discussed below.

Appellants next argue that it would not be obvious that Jepsen discloses a threshold voltage (Brief page 9, beginning with the second sentence at the top of the page). Jepsen discloses that the power source is a solar cell (abstract, lines 1-3; fig 2, “PV”). It would be obvious to one skilled in the art that a solar cell does not produce

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power (voltage or current) at night. Since there is no sunlight at night, there is no power for the Jepsen DC/DC converters (fig 2, item A) to convert. During daylight hours, the solar cell will begin to produce power. Once there is power to produce, the Jepsen converters can begin to provide power to the DC bus (item 3). The threshold is breached when the sun rises that the solar cell provides enough power to the DC/DC converter to allow it to function as a converter.

The Examiner admits that Jepsen does not use the word "threshold" with reference to the operation of the DC/DC converters. As discussed above, the solar cells do not provide power at night, but they do provide power during the day. Therefore, the Jepsen DC/DC converters are not active at night, while during the daytime they are active. Thus, a threshold voltage would be obvious. Since the claim was rejected under §103(a), it is not necessary that Jepsen explicitly disclose a threshold voltage.

The Examiner disagrees with appellants' characterization of Vinciarelli (Brief, pages 9-10, bridging paragraph). Appellants contend that the Vinciarelli model neglects "intrawinding capacitance." The Examiner admits that some intrawinding capacitance exists in the Vinciarelli circuit. Capacitance is defined as "1a: the property of an electrical nonconductor that permits the storage of energy as a result of separation of charge that occurs when opposite surfaces of the nonconductor are maintained at a difference of potential. 1b. the measure of this property that is equal to the ratio of the charge on either surface to the potential difference between the surfaces." (Merriam-Webster online dictionary; <http://www.merriam-webster.com/dictionary/capacitance>).

Capacitance will exist almost anywhere that two electrical conductors are placed near each other (“intrinsic capacitance”). Intrinsic capacitance can be minimized (for example, by shielding conducting wires with a magnetic resistant material such as rubber), but it can never be fully prevented. It is respectfully noted that appellants have pointed to the intrinsic capacitance of Vinciarelli without addressing appellants’ own design. Specifically, appellants do not describe in the specification or show in their figures how the DC/DC converters do not contain any intrinsic capacitance or how any of this intrinsic capacitance is prevented from buffering energy. It is noted that appellants’ figures do not show any internal features of the DC/DC converters (see also drawing objection, Final Rejection, April 7, 2009; pages 4-5).

Next, appellants contend that Vinciarelli’s figure 2 is only a circuit model, and “therefore cannot suffice for the disclosure of features of the system as claims.” Appellants’ have provided no support for their argument. Vinciarelli’s figure 2 was published and was available in the prior art (April 13, 1996) before appellants earliest filing date (December 21, 2004). Appellants’ arguments do not show how labeling this figure as “a model or construct” would disqualify it from the realm of prior art.

As support for the combination of references (Brief, page 10 beginning at line 7), the Examiner cited the reduction of parts. The art rejection, as cited by appellants’ (Brief, page 10, middle of the page), states that replacing both the Jepsen DC/AC converter and the AC/DC converter with one Vinciarelli DC/DC converter would reduce the number of parts of the device. This is because two converters are effectively

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replaced with one converter. With fewer components and less parts, the circuit is simplified.

Appellants' arguments consistently refer to replacing only the Jepsen DC/AC converter. This state misquotes the Examiner's art rejection of the claims. Appellants argue that the combination of reference will not result in the desired function of not buffering energy. As discussed in the §112(1) rejection, the art rejection of the claims will not treat the limitation of not buffering energy. Rather, the claims are interpreted as reciting that the DC/DC converters do not include capacitors. It is respectfully noted that the Examiner's reasons for combining references does not have to match the appellants' stated goal. The Examiner maintains that the references are properly combined.

Appellants have not provided any arguments regarding the patentability of claims 3-7 and 14-17, except to say that they depend from allowable independent claims. Claims 1 and 10-11 are not patentable over §112(1) because appellants have not demonstrated how to construct a DC/DC converter that does not buffer any energy. The claims are also not patentable §103 in view of Jepsen and Vinciarelli, since the references combine to disclose that it is known to construct a converter without capacitors.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

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Respectfully submitted,

Adi Amrany

/Adi Amrany/ Examiner, Art Unit 2836

Conferees:

/Jared J. Fureman/

Supervisory Patent Examiner, Art Unit 2836

/David S Martin/

Quality Examiner, T.C. 2800